HARDWARE OPEN SYSTEMS TECHNOLOGIES

Hardware Open Systems Technology (HOST)

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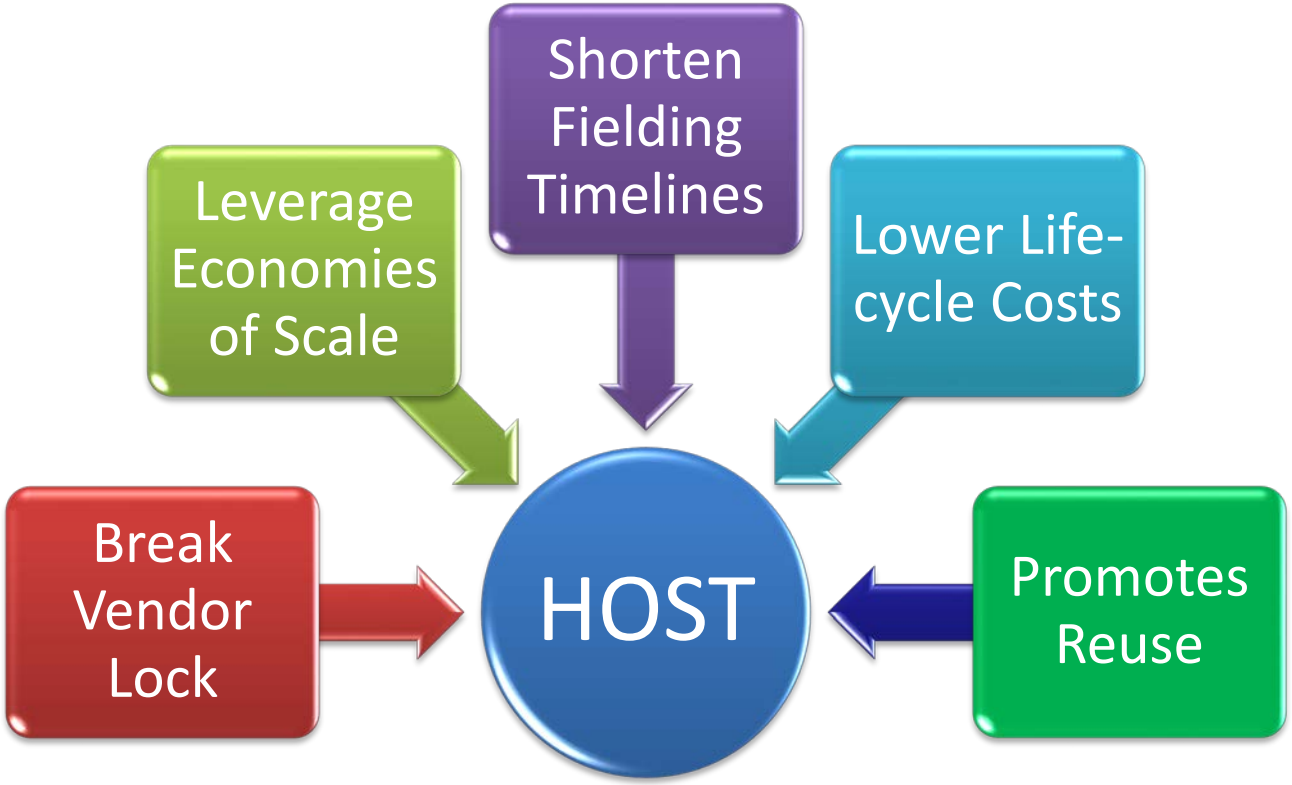
NAVAIR PMA209

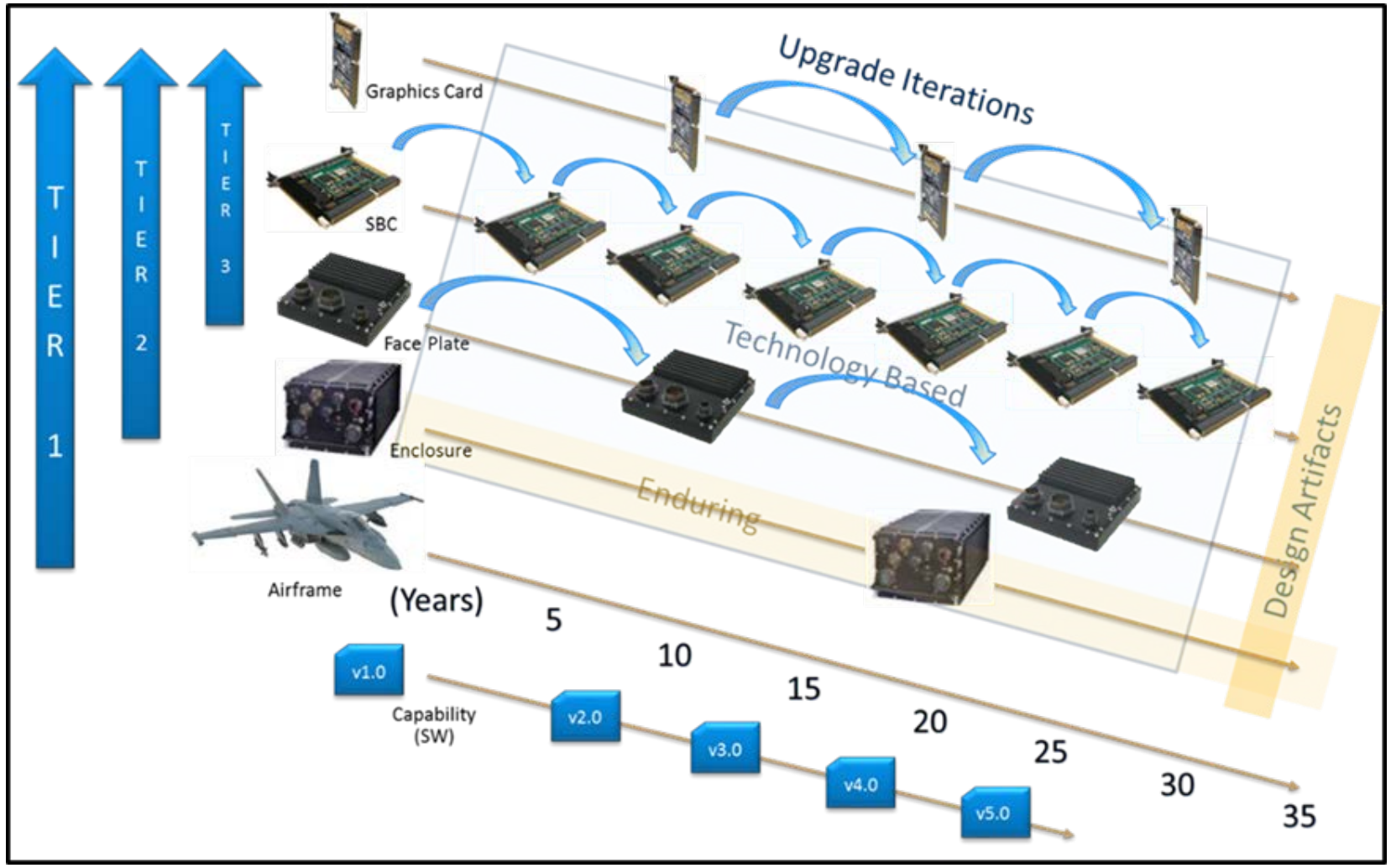
HOST – A Key Pillar of NAVAIR's Open Architecture Approach

Key Goals



"*Provides a framework for developing embedded computing systems for U.S. military platforms. HOST provides U.S. Government Acquisition, System Integrators, and Third Party HOST Component Vendors with an open, interoperable, upgradeable, and sustainable embedded system standard.*"

HOST Development Overview



HOST Benefits

Old Paradigm	New Paradigm
Circuit Card Assembly	HOST Assembly
Custom Functionality Defined by Integrator	Standardized Interfaces to Provide Functionality
Custom Set of Cards	Standardized Set of Cards
Inter Card Jumpers Complicates Wiring	Utilizes Defined Interfaces Over Back, and Mid Plane

The HOST Standards

TIER I: CORE TENETS (Single Document)

Preserve HOST "openness" by establishing universal requirements that apply to all HOST components regardless of core technology

TIER II: CORE TECHNOLOGIES (Document for each core technology chosen)

Define platform agnostic technical requirements for core technologies (Examples are OpenVPX, PC104, and VME)

TIER III: COMPONENT SPECIFICATIONS (Many Documents)

These are component level documents that will guide H/W development to facilitate modular components, Tier III reuse, and upgradeability

Tier 1 HOST Components

- HOST Components
  - Enclosures, Transmission Components, External Interfaces and Modules

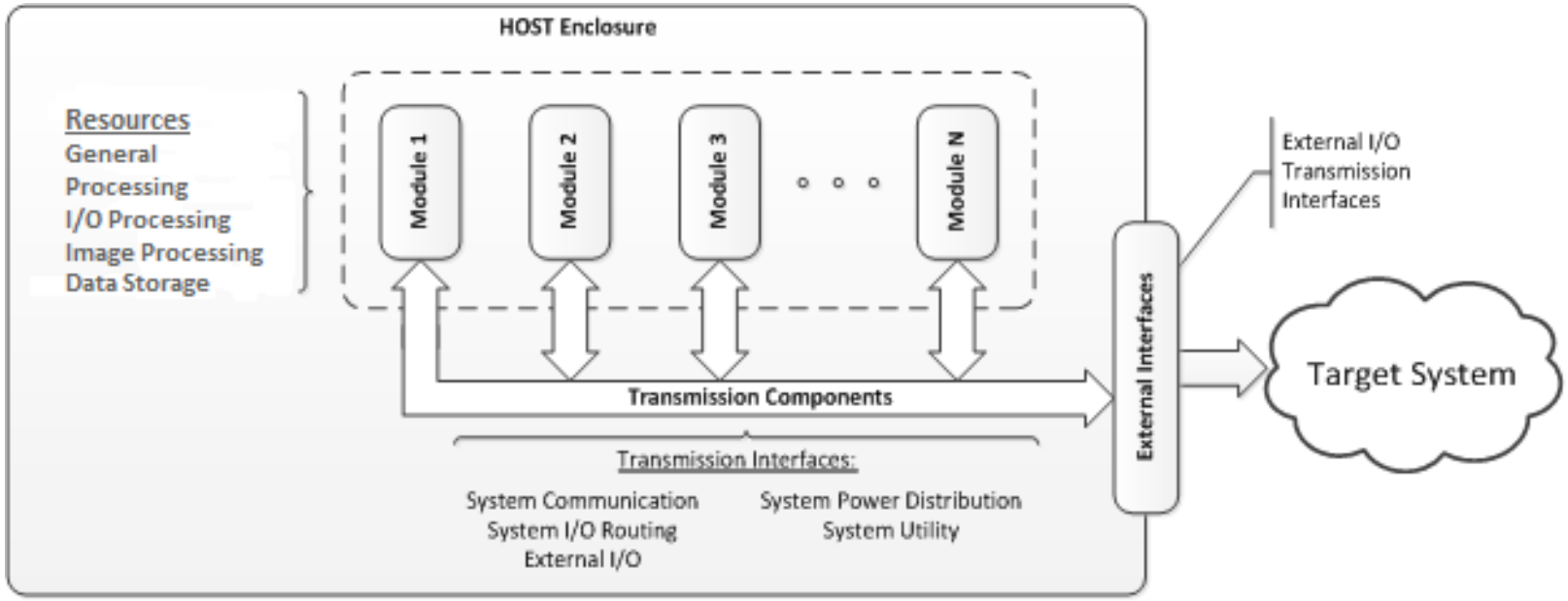
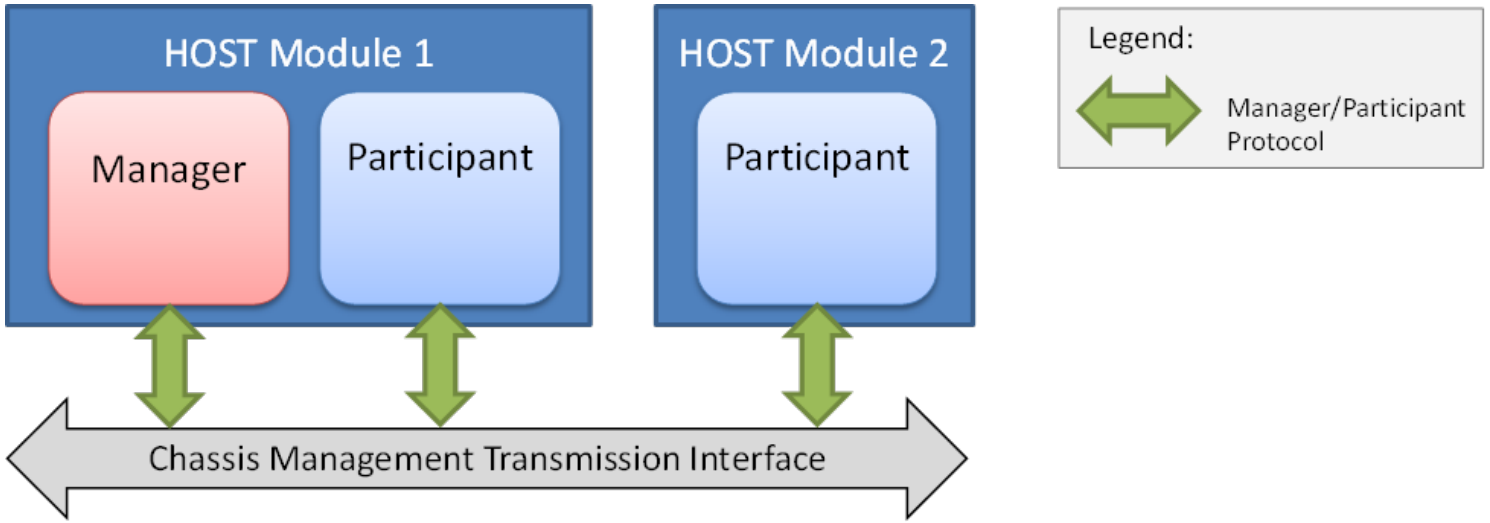


Figure 4-2 – Example HOST Component Categories

Tier 1 HOST-Management (HOST-MGMT)

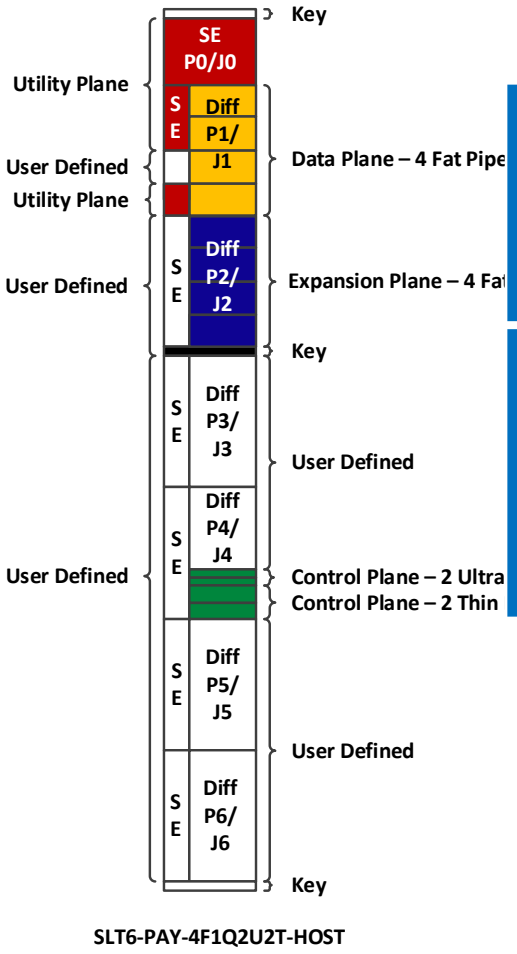


Autonomous subsystem that provides application independent hardware management and monitoring capabilities

Logical control elements for HOST-MGMT representation Managers (chassis-level) and Participants (module-level)

Manager/Participants Protocol (MPP) defines standardized means of data exchange

Tier 2 Payload Modules

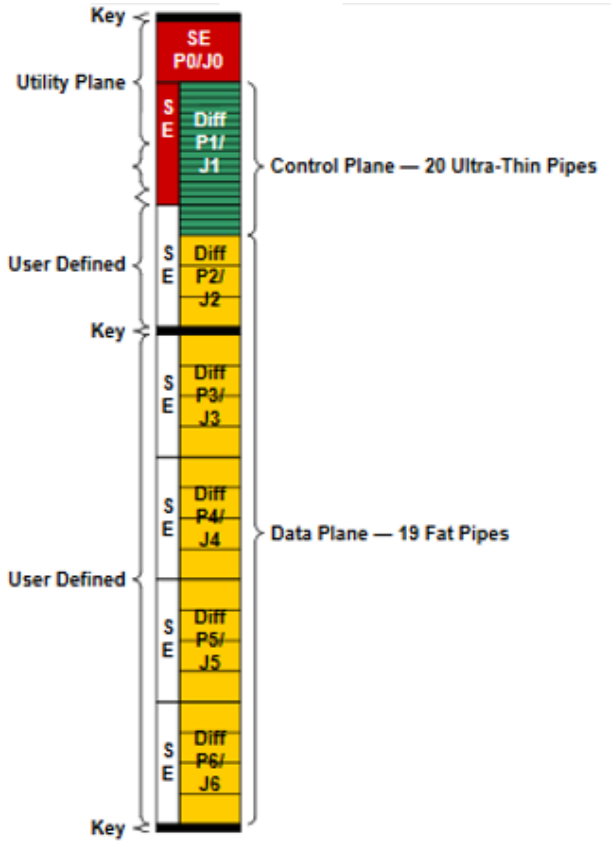


SLT6-PAY-4F1Q2U2T-HOST

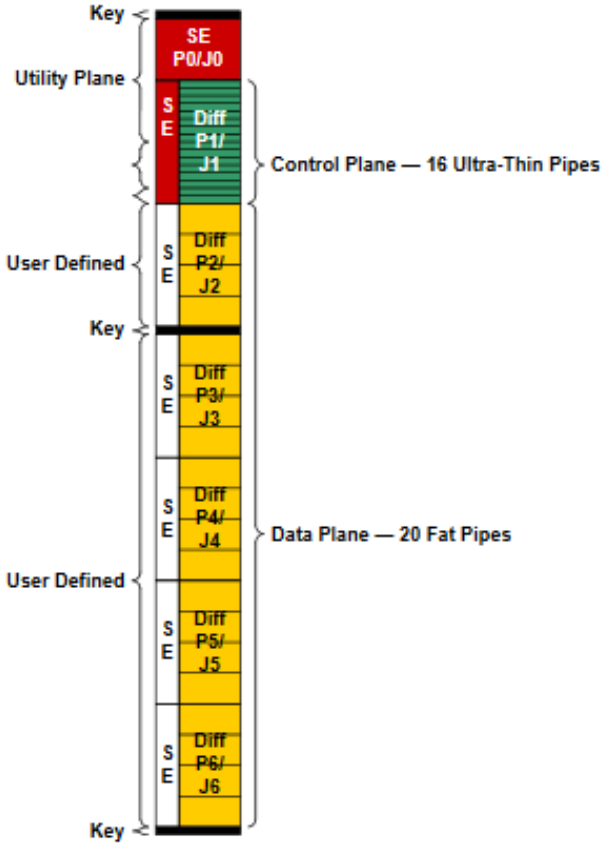
Profile Name	Data Plane 4 FP	Expansion Plane 4FP	Control Plane 2 UTPs		Control Plane 2 TPs	
	DP01 – DP04	DP01 –DP04	CPutp01	CPutp02	CPtp01	CPtp02
MOD6-PAY-4F1Q2U2T-HOST	10GBase-KX4 Ethernet per ANSI/VITA 65 Section 5.1.5	PCIe per ANSI/VITA 65-2010 Section 5.3	1000BASE-KX or BX per ANSI/VITA 46.6		1000BASE-T per ANSI/VITA 65-2010 Section 5.1.1	

T2-PER-0045: Payload Modules **may** implement 10GBASE-KR on the Control Plane UTPs.

Tier 2 Switch Modules



Profile 1



Profile 2

Tier 2 Payload Modules

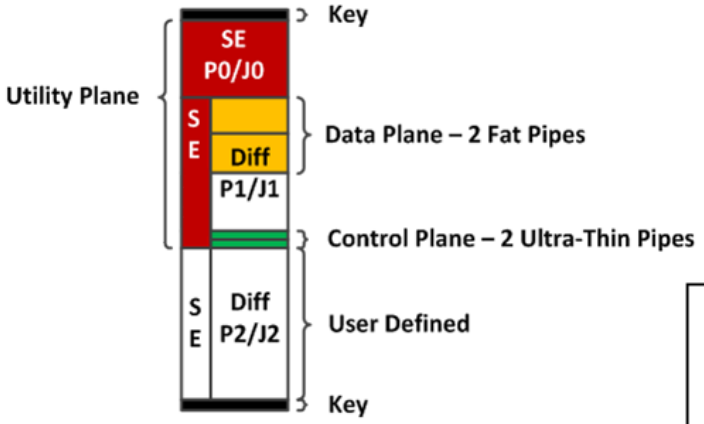
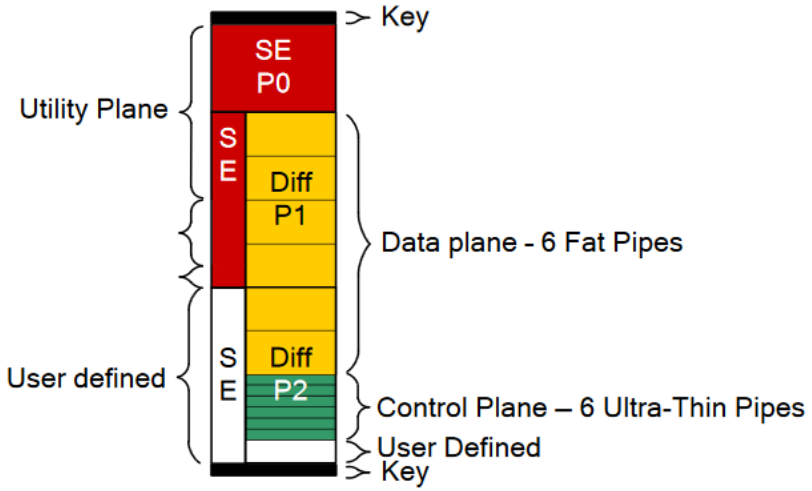


Figure 5-2 – HOST Payload Slot Profile, SLT3-PAY-2F2U-HOST

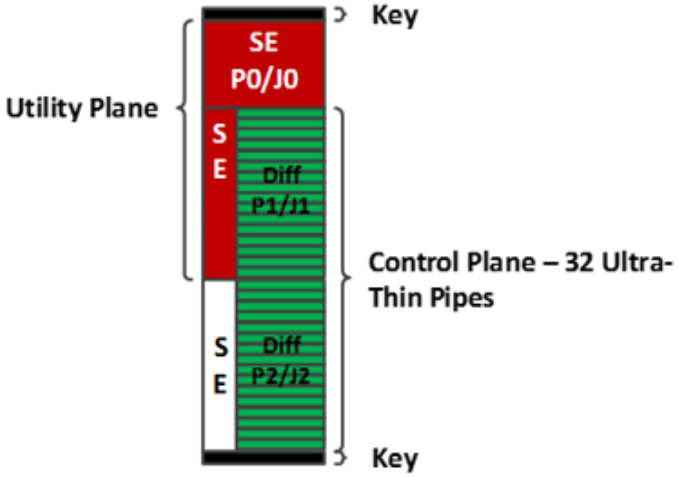
Profile Name	Data Plane 2 FP		Control Plane 2 UTPs	
	DP01	DP02	CPutp01	CPutp02
MOD3-2F2U-HOST	PCIe per ANSI/VITA 65-2010 Section 5.3		1000BASE-KX or BX per ANSI/VITA 46.6	

T2-PER-0045: Payload Modules **may** implement 10GBASE-KR on the Control Plane UTPs.

Tier 2 Switch Modules



Profile 1



Profile 2

Tier 2 Payload Modules

- Mezzanine Mapping
  - HOST calls out specific ANSI/VITA 46.9 I/O mapping for Payload Modules that have Mezzanine sites.
  - 46.9 calls out ways for Plug-In Modules to route I/O from their Mezzanine Sites to the backplane connector(i.e RT 2-R) wafers.

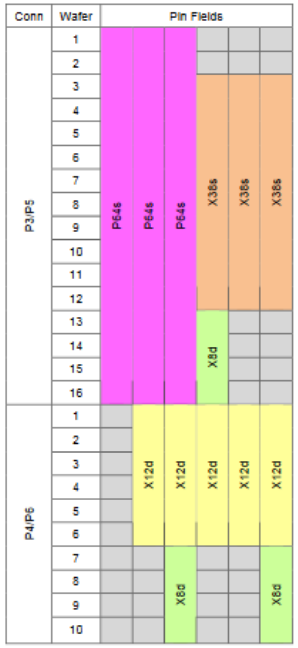


Figure 5-1: 6U VPX Carrier Backplane Pin Field Summary

From VITA46.9

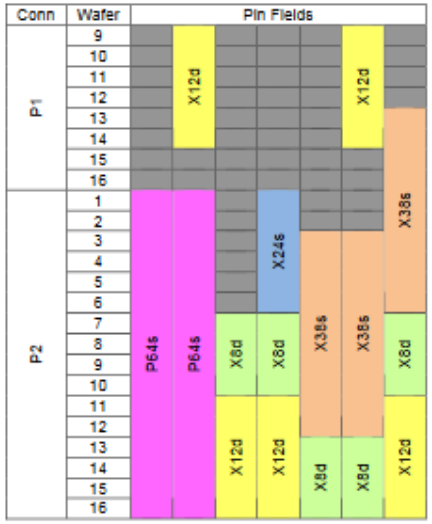


Figure 4-1: 3U VPX Carrier VITA 46.0 Connector Pin Field Summary

From VITA46.9

Questions